Amendments to the Claims

1-172. (Canceled)

173. (New) An electronic substrate having a plurality of semiconductor devices, comprising:

a substrate;

a thin film of nanowires, formed on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions; and

contacts formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices.

174. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises transistors, wherein said contacts comprise gate, source and drain electrodes formed above or below said thin film of nanowires, wherein said thin film of nanowires forms channels between said source and said drain electrodes.

175. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises diodes, and wherein said contacts comprise anode and cathode electrodes formed above of below said thin film of nanowires.

176. (New) The semiconductor devices of claim 175, wherein said thin film of nanowires forms a p-n junction between said anode and cathode electrodes.

177. (New) The semiconductor devices of claim 175, wherein said diodes comprise light emitting diodes.

178. (New) The semiconductor devices of claim 173, wherein at least a subset of the

semiconductor devices comprises logic devices.

179. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises memory devices.

180. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises an active matrix driving circuit.

181. (New) The semiconductor devices of claim 173, wherein said nanowires are aligned substantially parallel to their long axis.

182. (New) The semiconductor devices of claim 174, wherein the nanowires are aligned approximately parallel to an axis between the source and drain electrodes.

183. (New) The semiconductor devices of claim 174, wherein said gate electrodes are formed on the substrate, said thin film of nanowires is formed on said gate electrodes, and said source and said drain electrodes are formed on said thin film of nanowires.

184. (New) The semiconductor devices of claim 174, wherein said source and said drain electrodes are formed on said substrate, said thin film of nanowires is formed on said source and said drain electrodes, and said gate electrodes are formed on said thin film of nanowires.

185. (New) The semiconductor devices of claim 174, wherein said gate, source and drain electrodes are formed on said substrate, and said thin film of nanowires is formed on said gate, source and drain electrodes.

186. (New) The semiconductor devices of claim 174, wherein said gate, source and drain electrodes are formed on said thin film of nanowires.

187. (New) The semiconductor devices of claim 173, further comprising interconnects between a subset of the semiconductor devices.

188. (New) The semiconductor devices of claim 173, wherein said substrate comprises a flexible thin film.

189. (New) The semiconductor devices of claim 173, wherein said substrate comprises transparent material.

190. (New) The semiconductor devices of claim 173, wherein said substrate comprises a transparent material.

191. (New) The semiconductor devices of claim 173, wherein said nanowires are single crystal nanowires, wherein electric carriers transport through said single crystal nanowires with a mobility comparable to that of electric carriers transporting in a device formed from traditional planer single crystal semiconductor materials

192. (New) The semiconductor devices of claim 174, wherein said thin film of nanowires comprises a sufficient number of nanowires to have a on state current level in the channels of greater than 10 nanoamps.

193. (New) The semiconductor devices of claim 174, wherein said channels comprise more than one nanowire.

194. (New) The semiconductor devices of claim 174, at least a subset of said gate electrodes comprise more than one thin film of nanowires.

195. (New) The semiconductor devices of claim 174, wherein at least a subset of the channels comprises a p-n junction, whereby during operation the p-n junctions emit light.

196. (New) The semiconductor devices of claim 173, wherein said nanowires are doped.

197. (New) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped cores.

198. (New) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped shells.

199. (New) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped cores and shells.

200. (New) The semiconductor devices of claim 174, wherein at least a subset of said nanowires are oxidized to thereby form a gate dielectric.

201. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices are electrically coupled to another circuit.

202. (New) The semiconductor devices of claim 201, wherein said circuit is a logic circuit.

203. (New) The semiconductor devices of claim 201, wherein said circuit is a memory circuit.

204. (New) The semiconductor devices of claim 201, wherein said circuit is an active matrix driver circuit.

205. (New) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices are physically coupling to another circuit.

206. (New) The semiconductor devices of claim 205, wherein said circuit is a logic circuit.

207. (New) The semiconductor devices of claim 205, wherein said circuit is a memory circuit.

208. (New) The semiconductor devices of claim 205, wherein said circuit is an active matrix driver circuit.

209. (New) The semiconductor devices of claim 173, wherein said nanowires are patterned.

210. (New) The semiconductor devices of claim 209, wherein said patterned nanowires are photolithography patterned.

211. (New) The semiconductor devices of claim 209, wherein said patterned nanowires are screen printed.

212. (New) The semiconductor devices of claim 209, wherein said patterned nanowires are ink-jet printed.

213. (New) The semiconductor devices of claim 209, wherein said patterned nanowires are micro-contact printed.

214. (New) The semiconductor devices of claim 173, wherein the nanowires are spin casted.

215. (New) The semiconductor devices of claim 173, wherein the nanowires are mechanically aligned.

216. (New) The semiconductor devices of claim 173, wherein the nanowires are flow-

aligned.

217. (New) The semiconductor devices of claim 173, wherein the nanowires are shear-force aligned.

218. (New) The semiconductor devices of claim 173, wherein said nanowires comprise sufficient density to have statistic probability of achieving a device anywhere on the substrate.

219. (New) The semiconductor devices of claim 173, further comprising a layer of oxide deposited on at least a portion of said nanowires.

220. (New) The semiconductor devices of claim 173, wherein said nanowires are ballistic conductors having a mobility greater than that of single crystal semiconductor material.

221. (New) The semiconductor devices of claim 173, wherein said nanowires are randomly oriented.

222. (New) The semiconductor devices of claim 173, wherein said nanowires are a formed as a monolayer film, a sub monolayer film, or a multi layer film.

223. (New) The semiconductor devices of claim 174, wherein for at least one channel of said channels, a first end of at least two nanowires of said nanowires is electrically coupled with a first contact of said channel, and a second end of said at least two nanowires is electrically coupled with a second contact of said channel.

224. (New) A method of making an electronic substrate having a plurality of semiconductor devices, comprising:

(a) forming on a substrate a thin film of nanowires with a sufficient density of

nanowires to achieve an operational current level;

(b) defining a plurality of semiconductor device regions in the thin film of nanowires; and

(c) forming contacts at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices.

225. (New) The method of claim 224, further comprising aligning the nanowires substantially parallel to their long axis.

226. (New) The method of claim 224, wherein step (c) comprises forming source and drain electrodes, whereby the nanowires form a channel having a length between respective ones of the source and drain electrodes.

227. (New) The method of claim 226, further comprising a step of forming gate electrodes.

228. (New) The method of claim 224, wherein step (c) comprises forming anode and cathode electrodes.

229. (New) The method of claim 226, wherein the nanowires are aligned approximately parallel to an axis between the source and drain contacts

230. (New) The method of claim 227, wherein the gate electrodes are formed on the substrate, the thin film of nanowires is formed on the gate electrodes, and the source and drain electrodes are formed on the thin film of nanowires.

231. (New) The method of claim 227, wherein the source and drain electrodes are formed on the substrate, the thin film of nanowires is formed on the source and drain electrodes, and the gate electrodes are formed on the thin film of nanowires.

232. (New) The method of claim 227, wherein the gate, source and drain electrodes

are formed on the substrate, and the thin film of nanowires is formed on the gate, source and drain electrodes.

233. (New) The method of claim 227, wherein the gate, source and drain electrodes are formed on the thin film of nanowires.